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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 09/452,691      | 12/02/1999  | FRED D. BAILEY       | TI-27935            | 1638             |

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EXAMINER

FENTY, JESSE A

ART UNIT PAPER NUMBER

2815

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/452,691

Applicant(s)

BAILEY ET AL.

Examiner

Jesse A. Fenty

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-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8, 17 and 18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 17 and 18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 5) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 6) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/15/02 has been entered.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-3, 6, 7, 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Saia et al. (U.S. Patent No. 5,874,770).

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In re claims 1 and 17, Saia (Figs. 5, 12) discloses a semiconductor device, comprising:

- A lower metal interconnect layer (46) located over a semiconductor body (45);
- A multi-level dielectric layer (42, 10, 40) located over said lower interconnect layer;
- An upper metal interconnect layer (56) located over said multi-level dielectric layer; and
- A thin film resistor (28) embedded within said multi-level dielectric layer between and physically separated in a vertical direction from said lower metal interconnect layer and said upper metal interconnect layer.

In re claims 2 and 18, Saia discloses the devices of claims 1 and 17 respectively, further comprising:

- A first plurality of conductively filled vias (47) extending from said upper metal interconnect layer to said lower interconnect layer; and

- A second plurality of conductively filled vias (21, 52) extending from said upper metal layer to said thin film resistor.

In re claim 3, Saia discloses the device of claim 1, wherein said thin film resistor comprises a top plate which can be used as a hard mask (MacElwee; column 7, lines 48-51, teaches the use of a top electrode plate as a hard mask.)

In re claim 6, Saia discloses the device of claim 1, wherein said thin film resistor structure comprises TaN (column 5, line 7).

In re claim 7, Saia discloses the device of claim 1, wherein said thin film resistor structure comprises SiCr (column 5, line 9).

*Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 4, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saia et al. as applied to claim 1 above, and further in view of Linn et al. (U.S. Patent No. 5,547,896).

In re claims 4 and 5, Saia discloses the device of claim 3, wherein the resistor comprises chromium silicide (column 5, line 9) with a masking layer but does not expressly disclose a "hard mask" layer comprising TiW or TiN. Linn et al. (Figs. 1a-3b) discloses an electrode of the same material overlaid by a TiW or TiN "hard mask." It would have been obvious to one skilled in the art at the time of the invention to use a hard mask as taught by Linn to overlay the chromium electrode of Saia for the purpose, for example, of cleanly etching a chromium alloy resistor such that residual contaminants will not compromise the integrity of the chromium resistor (Linn; column 1, lines 60-66; column 2, lines 26-30).

In re claim 8, Saia discloses the device of claim 3, but does not expressly disclose the resistor comprising NiCr. Linn discloses a thin film resistor comprising NiCr. It would have been obvious for one skilled in the art at the time of the invention substitute the SiCr resistor of Saia with the NiCr resistor as disclosed by Linn because Linn discloses said materials are "well known" and commonly used thin film transistor structures (column 1, lines 9-13).

*Response to Arguments*

4. Applicant's arguments filed 07/22/02 have been fully considered but they are not persuasive.

In response to applicant's argument regarding claim 1 that Saia does not disclose or suggest a thin film resistor embedded within a multi-level dielectric layer between and physically separated in a vertical direction from a lower metal interconnect layer and an upper metal interconnect layer; Examiner more clearly defines, as is explained in the above rejection, the thin film resistor (28) embedded within the dielectric layer as claimed in the amended claims.

*Conclusion*

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Boyd et al. (U.S. Patent No. 5,352,923) discloses a trench resistor structure relevant to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 703-308-8137. The examiner can normally be reached on 5/4-9 1st Fri. Off.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-746-3892 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Jesse A. Fenty  
Examiner  
Art Unit 2815

JAF  
September 30, 2002



EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
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